

REMARKS

Claims 1-20 remain in the present application. Applicants respectfully request further examination and reconsideration of the rejections based on the amendments and arguments set forth below.

Claim Rejections – 35 U.S.C. §103

Claims 1-3, 6, 10-11 and 15-16

Claims 1-3, 6, 10-11 and 15-16 are rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent Number 5,994,937 to Hara et al. (hereafter referred to as "Hara"), in view of United States Patent Number 5,926,045 to Kwon (hereafter referred to as "Kwon"), and further in view of United States Patent Number 6,031,366 to Mitsuishi (hereafter referred to as "Mitsuishi"). Applicants have reviewed the cited references and respectfully assert that the embodiments of the present invention as recited in Claims 1-3, 6, 10-11 and 15-16 are not rendered obvious by Hara in view of Kwon, and further in view of Mitsuishi for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 1, which recites a timer circuit comprising (emphasis added):

an output stage coupled to a configurable delay element, wherein said configurable delay element comprises a plurality of selectively-activated components operable to adjust a delay through said timer circuit; and

a pull-down path coupled to said output stage and comprising a circuit for providing a selectable amount of pull down current, said pull-down path also coupled to receive a reference signal that varies in proportion to temperature and wherein said delay through said timer circuit is inversely proportional to said temperature.

Independent Claim 10 recites similar limitations to independent Claim 1. Claims 2-3, 6, 11 and 15-16 depend from their respective independent claims and recite further limitations to the claimed invention.

Applicants respectfully assert that Hara fails to teach or suggest the limitation of “an output stage” as recited in independent Claim 1. As recited and described in the present application, an output stage is coupled to a configurable delay element, where the output stage provides a *output* signal.

In contrast to the claimed embodiments, Applicants understand the cited portion of Hara to teach transistors that receive a delay *input*. For example, Hara teaches that transistors 410 and 412 receive a delay input (Figure 4). As such, Hara teaches away from the claimed embodiment by teaching transistors that receive a delay *input* instead of an output stage providing an *output* signal as claimed.

Applicants respectfully submit that both Kwon and/or Mitsuishi, either alone or in combination with Hara and/or one another, fail to cure the deficiencies of Hara discussed above with respect to independent Claim 1. Specifically, Applicants respectfully submit that Kwon and Mitsuishi also fail to teach or suggest the limitation of “an output stage” as recited in independent Claim 1.

Additionally, Applicants wish to respectfully remind the Examiner that a proposed modification under 35 U.S.C. §103(a) cannot render the prior art unsatisfactory for its intended purpose, and also cannot change the principle of operation of a reference (MPEP §2143.01). Hara teaches a pulse generator with “a delay element that provides consistent delay by compensating for process and power supply voltage variations that would normally change the delay” (emphasis added) (col. 3, lines 11-14). As such, Applicants respectfully submit

that replacing Hara's transistors 414 and 424 with Mitsubishi's current source shown in Figure 3 of Mitsubishi would provide *inconsistent* delay to Hara's pulse generator, thereby rendering it unsatisfactory for its intended purpose as well as changing its principle of operation. Furthermore, Applicants respectfully submit that such a modification would require a substantial redesign of Hara's circuit (e.g., adding many components, adding control circuitry to control the switches, etc.), thereby further showing that the teachings of Hara and Mitsubishi are not sufficient to render the Claims *prima facie* obvious (MPEP §2143.01; *In re Ratti*, 270 F.2d at 813, 123 USPQ at 352 (CCPA 1959)).

Furthermore, Applicants respectfully submit that no suggestion or motivation to combine Hara and Mitsubishi in the claimed fashion has been shown sufficiently to establish a *prima facie* case of obviousness, as discussed in MPEP §2143. Page 3 of the rejection states that one of ordinary skill in the art would be motivated to combine Hara and Mitsubishi in the claimed fashion to save cost. However, as discussed above, such a combination would add a significant number of circuit elements and may also require additional circuitry to control the switches. As such, replacing Hara's transistors 414 and 424 with the current source taught in Figure 3 of Mitsubishi would *add significant cost* to Hara's circuit instead of reducing cost as suggested by the rejection. Consequently, Applicants respectfully submit that one of ordinary skill in the art would not be motivated to combine Hara and Mitsubishi in the claimed fashion.

For these reasons, Applicants respectfully submit that independent Claim 1 is not rendered obvious by Hara in view of Kwon, and further in view of Mitsubishi, thereby overcoming the 35 U.S.C. §103(a) rejections of record. Since independent Claim 10 recites limitations similar to those discussed above with

respect to independent Claim 1, independent Claim 10 also overcomes the 35 U.S.C. §103(a) rejections of record. Since Claims 2-3, 6, 11 and 15-16 recite further limitations to the invention claimed in their respective independent claims, Claims 2-3, 6, 11 and 15-16 also overcome the 35 U.S.C. §103(a) rejections of record. Therefore, Claims 1-3, 6, 10-11 and 15-16 are allowable.

Claims 1-20

Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hara in view of Kwon, further in view of Mitsuishi, and further in view of United States Patent Number 6,388,490 to Saeki (hereafter referred to as "Saeki"). Applicants have reviewed the cited references and respectfully assert that the embodiments of the present invention as recited in Claims 1-20 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki for the following reasons.

Applicants respectfully submit that both Saeki, either alone or in combination with Hara, Kwon and/or Mitsuishi, fail to cure the deficiencies of the Hara/Kwon/Mitsuishi combination discussed above with respect to independent Claim 1. Specifically, Applicants respectfully submit that Saeki also fail to teach or suggest the limitation of "an output stage" as recited in independent Claim 1.

Applicants respectfully direct the Examiner to independent Claim 17, which recites a method of varying a delay of a timer circuit comprising (emphasis added):

during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit;

during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down

path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage; and
during operation of said timer circuit, varying a reference signal coupled to said pull down path to vary delay through said timer circuit inversely proportional to temperature of said timer circuit.

Claims 18-20 depend from independent Claim 17 and recite further limitations to the claimed invention.

Applicants respectfully submit that Hara fails to teach or suggest the limitation of a “during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit” and “during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage” as recited in independent Claim 17. As recited and described in the present application, a configuration stage and operation stage of the timer circuit exist. During the configuration stage, configuration bits are set to control the delay through the timer circuit by determining an amount of elements coupled to the output stage of the timer circuit. Additionally, a second set of configuration bits are set during configuration to control an amount of pull-down current of the timer circuit.

In contrast to the claimed embodiments, Applicants respectfully assert that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest separate configuration and operation stages of a timer circuit. Further, the cited combination also fails to teach or suggest setting *two sets of configuration bits* during configuration to control *both* the delay of the output stage and an amount of pull-down current of the timer circuit.

For these reasons, Applicants respectfully assert that independent Claim 17 is not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki, thereby overcoming the 35 U.S.C. §103(a) rejections of record. Since Claims 4-5, 7-9, 12-14 and 18-20 recite further limitations to the invention claimed in their respective independent claims, Claims 4-5, 7-9, 12-14 and 18-20 also overcome the 35 U.S.C. §103(a) rejections of record. Therefore, Claims 4-5, 7-9, 12-14 and 17-20 are allowable.

CONCLUSION

Applicants respectfully submit that Claims 1-20 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Dated: 4/23, 2007

BMF

Bryan M. Failing
Registration No. 57,974

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060